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A zero-crossing based 10-bit 100 MS/s pipeline ADC with controlled current in 90 nm CMOS

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Abstract In this paper, a new charging technique for low power zero-crossing based circuit pipeline analog-to-digital converters (ADCs) is presented. The charging current sources are implemented as voltage-controlled current sources in order to charge the sampling capacitors based on the error signal. Using this method, the ADC power consumption is reduced while improving the accuracy. The necessary current control block is shared between consecutive stages further reducing the power consumption and die area. The proposed technique is applied to a 10-bit 100 MS/s pipeline ADC designed in a 90 nm CMOS technology with 1 V power supply. Circuit level simulation results using Cadence Spectre show a signal-to-noise and distortion ratio of 55.6 dB with 3.56 mW power consumption resulting in a figure of merit of 72.3 fJ/conv.step without employing any calibration technique.

Keywords Pipeline analog-to-digital converters · Zero-crossing based circuits · Switched-capacitor circuits

1 Introduction

Digital communication applications require analog-to-digital converters (ADCs) with high resolution and several megahertz of input signal bandwidth. Pipeline ADCs are commonly used for such applications and are considered to be one of the most popular ADC architectures. Such ADCs have different applications such as imaging, communications, displays and television receivers [1]. Today, these ADCs are used in many handheld devices such as smartphones and tablets bringing with it an added emphasis on reduced power consumption. Recent technological advances and newer CMOS technology nodes have made switched-capacitor circuits much more appealing [2]. However, these same advances have created challenges for analog designers. Limitations such as the reduced voltage headroom and intrinsic device gain along with the increased leakage and mismatches force the designer to increase the power consumption to meet the required specifications [3].

Due to their multi-stage nature, pipeline ADCs require gain stages between consecutive stages to work properly. In the 1.5 bit/stage implementation of these ADCs, the required gain is two. These gain stages are conventionally implemented by using switched-capacitor circuits with an operational amplifier, creating the gain using the charge transfer between the capacitors. To achieve the required amount of accuracy for present applications, the operational amplifiers need strict specifications which are usually satisfied by increasing the ADC's overall power consumption [4]. But, this might be impossible to implement in future technology nodes. This is why the recent efforts have been focused to replace the amplifier with circuits that can simulate the required gain with much less power consumption.

These efforts have been successful in creating several methods to replace the operational amplifier. Open-loop amplification is one such method, which uses a much simpler open-loop gain stage along with advanced calibration methods to make up for reduced accuracy [5, 6]. Another method uses capacitive charge pumps to simulate the required stage gain [7, 8]. Using comparator-based switched capacitor circuits (CBSC) [9] is another method to replace the opamp with a comparator that turns charging current sources on or off based on node voltages to simulate the required gain. Another technique which is based on the CBSC method is zero-crossing based circuits (ZCBC) [10] which uses a very simple

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dynamic zero-crossing detector (DZCD) instead of the multi-stage comparator used in the CBSC. This method has been successful in effectively reducing the power consumption. However, constant current sources charge node voltages in a ramp causing the DZCD's delay to affect the accuracy. Also the current source will continue providing constant current and charging the nodes until the end of the charge transfer phase even after the node voltages have passed their final values. This increases the power consumption.

In recent years, different methods have been proposed resulting from the CBSC and ZCBC techniques. In [11], the CBSC technique is employed to replace the source-follower used in the capacitive charge-pump ADC proposed in [7], as the unity gain buffer. This has improved the overall ADC gain accuracy and increased the output swing [11]. In [12], the time-shifted correlated double sampling technique is used to mitigate the overshoot error in the CBSC method. In [13], the split-correlated level shifting (Split-CLS) technique is used alongside the ZCBC method. The split-CLS technique is based on using two operational amplifiers where one amplifies the input signal and the other reduces the gain error. The main amplifier is implemented using the ZCBC method and the error is reduced using a precise operational amplifier [13]. In [14], a time-domain ADC has been proposed. The required voltage to pulse width converters for this technique have been realized using the ZCBC technique [14]. However, most of these variations are based on using the CBSC and ZCBC techniques in their original form to improve other previously available methods and less work has been done to fix the issues limiting the CBSC and ZCBC techniques' performance.

In this work, a new charging method based on controlled current sources is proposed for ZCBC pipeline ADCs. As an example, a 10-bit 100 MS/s pipeline ADC is designed in a 90 nm CMOS process achieving a signal-to-noise and distortion ratio (SNDR) of 55.6 dB with 3.56 mW power consumption. The designed ADC achieved a figure of merit (FoM) of 72.3 fJ/conv.step showing an effective improvement on the original ZCBC design.

The paper is organized as follows. In Sect. 2, the structure of the original ZCBC method is briefly reviewed. The scheme of the proposed technique and its system level design are presented in Sect. 3. Section 4 presents the circuit level design of the proposed ADC with the new charging method. The circuit level simulation results are provided in Sect. 5. Finally, Sect. 6 concludes the paper.

2 Structure of the original ZCBC method

2.1 Behavioral description

The ZCBC stage as presented in [10] has the general structure depicted in Fig. 1. It is based on simulating the opamp-based gain stage's behavior. In the opamp-based circuit, the opamp forces the virtual ground condition while in the CBSC and ZCBC methods; this condition is detected by the comparator and DZCD, respectively.

During the sampling phase, ϕ_1, the input, V_{in}, is sampled on capacitors C_1 and C_2 which are chosen equally for 1.5 bit/stage applications. At the beginning of ϕ_2, there is a pre-charge phase, ϕ_{2I}, during which V_{out} is shorted to the ground. This resets the output. At the same time, $\bar{\phi}_{2I}$ turns M_2 on which pulls V_P up, turning on the next stage's sampling switch (M_3) [10]. Once ϕ_{2I} ends, V_X and V_{out} are released and start to ramp up due to I_1's constant current. Ramping continues until V_X gets high enough to turn M_1 on, pulling V_P down and turning M_3 off. This determines the next stage's sampling instant. To simulate the charge transfer behavior of the opamp-based gain stage, M_3 must be switched off once V_X reaches V_{CM}. Therefore, the DZCD must be adjusted to switch its output at the right moment by choosing M_1 and M_2's dimensions properly. Once the sampling switch is opened, the proper output value will be stored on C_L and it can be used by the next stage [10]. However, the current source is still active and will continue charging the nodes until the end of ϕ_2. V_X, V_{out} and V_Z will continue to ramp up until V_{out} is large enough to saturate the current source.

It should also be noted that when V_P is left to float after the pre-charge phase, the gate-drain capacitor of M_1 will transfer a signal-dependent charge to V_P which will cause a signal-dependent delay for the DZCD as M_1 also has to drain this added charge. To fix this problem, $\bar{\phi}_{2I}$ is used as shown in Fig. 1 to provide a biasing voltage to the gate of M_2 while V_X is charging. This will cause the extra charge to be drained via M_2.

In the ZCBC technique, the value of V_{out} at the end of the charge transfer phase is not the actual output voltage as is the case in conventional opamp-based stages. Therefore, the conventional comparator-based sub-ADCs cannot be used in their original form. Bit extraction is achieved by using bit-decision flip-flops. These flip-flops store the value of V_P at specific instants dictated by bit decision clock phases (ϕ_{BD}). These phases are created using a voltage-controlled delay line (VCDL) which uses a replica ZCBC stage to detect the instant that V_P would be set to zero for 0.25 V_{ref} input. This is the same instant when the flip-flops store the value for V_P. Therefore, if the input in the main stage is larger than 0.25 V_{ref}, the flip-flop stores a high value, as V_P has not yet been set to zero, whereas if the input is smaller than 0.25 V_{ref}, a low value is stored. Thus, the flip-flop will provide the value of the most significant bit extracted from the stage. By using another flip-flop with a phase set in the same way as before, but with $-0.25\ V_{ref}$ input for its replica stage, the other bit can also be extracted [10].

In this manner, the opamp-based circuit's behavior is simulated with very low power consumption and very

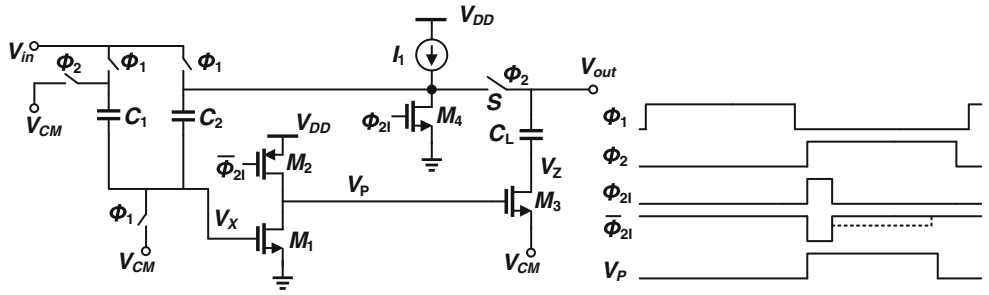

Fig. 1 Single stage of the original ZCBC design [10]

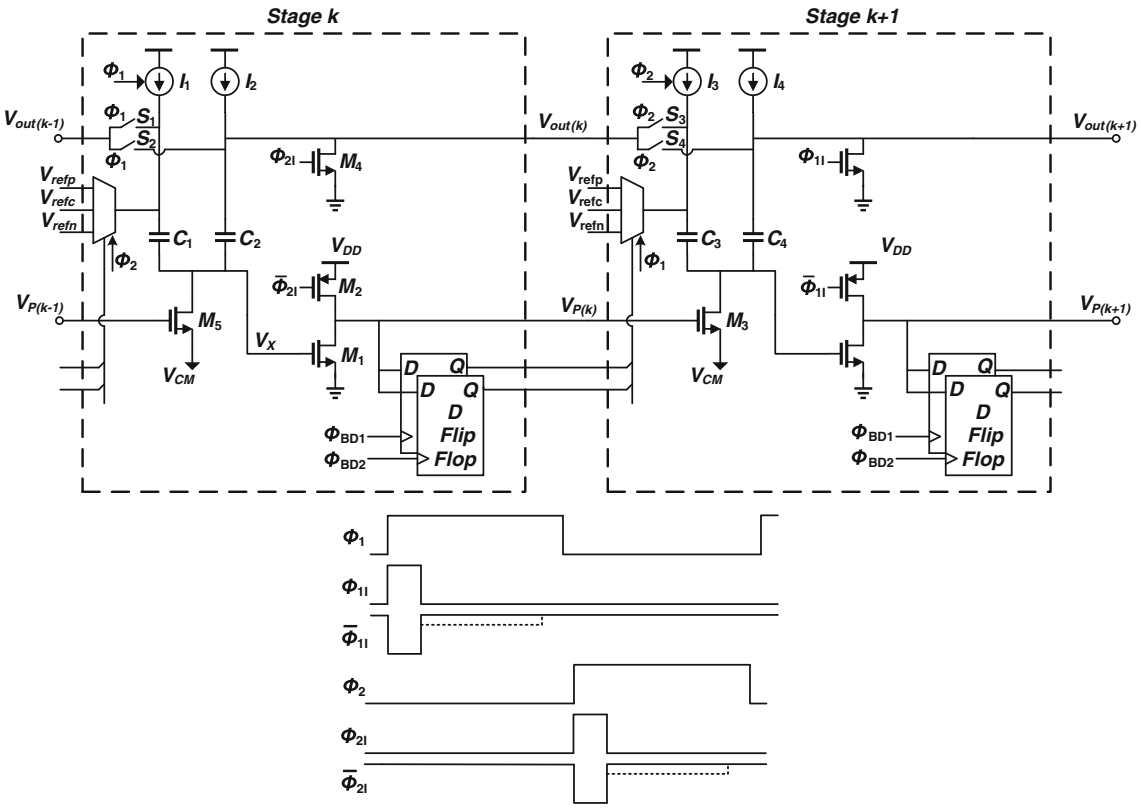

Fig. 2 General consecutive stages in the original ZCBC design [10]

simple circuitry. Obviously the results of this method will not be as accurate as when a precise and power hungry opamp is used. However, the reduced power consumption, area, and complexity make this an attractive method.

2.2 Circuit implementation

Section 2.1 provided an overview of the ZCBC method based on a simple circuit example. For the actual circuit implementation, some changes need to be made in the circuit shown in Fig. 1. Figure 2 presents two general consecutive pipeline stages as well as the required clock phases, using the original ZCBC method [10]. The current sources have been divided and split to remove the switch S from Fig. 1 and avoid the nonlinearity and swing limitations caused by the current passing through its on-resistance. Switches $S1$-$S4$ in Fig. 2 are used as shorting switches to remove the effects of current source mismatches. The rest of the circuit behaves as described in Sect. 2.1.

As described in Sect. 2.1, the conventional comparator-based sub-ADCs cannot be used in their original form for the ZCBC technique. In [15], traditional methods are implemented by using V_P also to control the sub-ADC. In

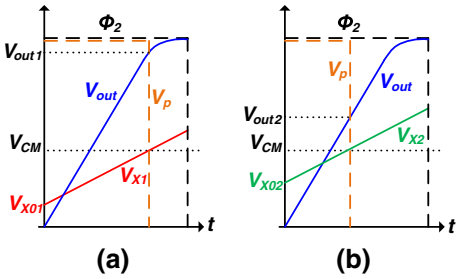

Fig. 3 Voltage behavior of the original ZCBC design: **a** for V_X with an initial value far from V_{CM} and **b** for V_X with an initial value close to V_{CM}

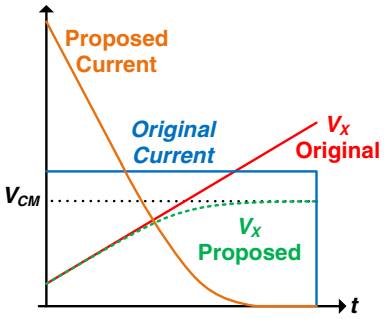

Fig. 4 Comparison of voltage and current behavior of the original ZCBC and the proposed method

[10], bit-decision flip-flops have been adopted as they also remove the need to match the MDAC and the sub-ADC paths' time constants.

3 Proposed charging technique

In the original ZCBC implementation, once V_X reaches V_{CM}, the DZCD (M_1 and M_2 in Fig. 2) sets its output to low and opens the sampling switch (M_3). This is called the sampling instant. V_X and V_{out} will continue to ramp after this instant until the end of the charge transfer phase. But, there is no need for the current to be applied to the circuit after the sampling instant. The sampling instant changes based on the input signal sampled during the sampling phase. An example of different sampling instants for different input signals is shown in Fig. 3. Figure 3(a) depicts a situation with a small initial value for V_X which in turn causes the necessary charging time to increase leading to a sampling instant closer to the end of the charging phase. Figure 3(b) displays a different situation where the initial value for V_X is larger. This decreases the necessary charging time leading to an earlier sampling instant. In such cases, the unnecessary current is applied to the circuit for more than half of the charge transfer phase resulting in more power consumption.

The charging technique proposed in this work is based on voltage controlled current sources (VCCS). These current sources are to be controlled by the difference between V_X and V_{CM}. This will cause the current to be at its largest amount in the beginning of the charge transfer phase and to decrease as V_X is increased. Once V_X reaches the vicinity of V_{CM}, the current will have a very low amount and finally be zero once V_X reaches V_{CM}, causing V_X to settle on V_{CM} and V_{out} on its proper final value by the end of the charge transfer phase. Therefore, using VCCS as proposed will reduce the power consumption by turning the current sources off once the final value of V_{out} is reached.

Using the proposed method will also improve the ADC accuracy. As reported in [10], the actual gain of the ZCBC stage, when including the effects of finite output impedance in the current sources and finite delay in the DZCD, is calculated as follows:

$$V_{out} = \frac{2}{1 + \frac{\Delta V_{out}}{V_A}} V_{in} \tag{1}$$

where V_A is the Early voltage of the current sources and ΔV_{out} is the amount of overshoot caused by the DZCD delay. This overshoot is defined as:

$$\Delta V_{out} = \alpha t_d \tag{2}$$

where α is the slope of V_X's charging ramp and t_d is the finite delay of the DZCD. When the current is controlled as proposed in this work, this slope (α) will be close to zero when V_X approaches V_{CM}, and therefore, the effect of the DZCD's finite delay is mitigated, bringing with it an increased gain accuracy. A comparison of the original ZCBC voltage and current waveforms and the ones proposed in this work is presented in Fig. 4.

Another benefit resulting from this technique is improved conditions for potential on-chip reference voltage implementations used to provide the voltage levels in each stage's DAC and also the biasing voltages. These reference voltages must settle within the pre-charge phase and they must hold a constant voltage value to within an LSB of precision when any given stage switches off and the current load changes. Using the proposed method means very low current levels during such changes which will relax the requirements on reference voltage circuits.

In order to test the benefits of the proposed method, an ideal VCCS was initially used as the charging current source for the original ZCBC design. The VCCS is set to be controlled by the error signal, (V_{CM}–V_X), with a transconductance of 3 mA/V. The DZCD was used to turn off the current source once V_X reaches V_{CM} and the sampling switch can now be controlled by ϕ_2 (charge transfer phase) as V_{out} has settled to its final value before the end of ϕ_2 and does not continue ramping as it did in the original design. This also simplifies the design of the sub-ADC, as the

output value will remain unchanged until the end of the transfer phase once the DZCD turns the current source off. Therefore, there is no more a need to use bit decision flip-flops as in [10] or to control the sub-ADC with the output of the DZCD as in [15], and the next stage's sub-ADC can be implemented conventionally as in [4]. The ideal implementation showed improved results by achieving 62 dB SNDR.

4 Circuit level design

4.1 Single-stage design

The proposed method is tested on a ZCBC pipeline ADC implementation. The converter is designed in a 90 nm CMOS technology and consists of eight pipeline stages each generating one effective bit followed by a 2-bit flash ADC as the backend providing a total of 10-bit output. The circuit operates at a sampling frequency of 100 MHz with a 1 V power supply. The input signal is a single-ended sine wave with 0.6 V peak-to-peak and 48 MHz frequency. Firstly, the design of a single pipeline stage is discussed followed by the multi-stage implementation description.

4.1.1 Current control block

In order to control the current as described in Sect. 3, a VCCS has to be used. One possible implementation of this is illustrated in Fig. 5 which is based on a simple differential pair. The current resulting from V_X is mirrored on M_{31}. The difference between this current and the one resulting from V_{ref} passes through M_{32} and is mirrored on M_I. Therefore, as the difference between V_X and V_{ref} is reduced, the output current will also be reduced. By selecting the value of V_{ref} and transistor dimensions carefully, the output current will be very close to zero once V_X reaches V_{CM}. The output of the DZCD (V_P) is used to turn off the current source through S_1 and S_2 switches in Fig. 5 to make sure V_X and V_{out} will remain constant once the virtual ground condition is met. At the beginning of the charge transfer phase, V_P is high, and therefore, M_I is connected to the current control block (CCB) through S_1. But, when V_X reaches its final value, V_P will fall, and therefore, S_1 will open and S_2 which is controlled by the NOT of V_P will be closed, connecting M_I's gate to V_{DD} and setting the output current to zero.

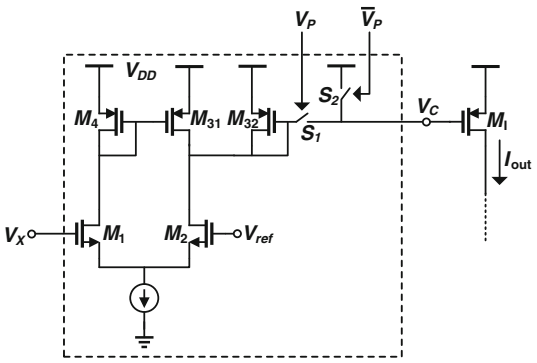

Fig. 5 Voltage controlled current source implementation as the current control block (CCB)

4.1.2 General pipeline stage

Figure 6(a) shows two general consecutive pipeline stages as used in this work with the required clock phases illustrated in Fig. 6(b). In contrast with Fig. 2 which depicts the original ZCBC implementation, the sampling switches are now controlled by the original stage phases instead of the output of the DZCD; the current sources are controlled using the CCBs and conventional sub-ADC implementations are used. Conventional dynamic comparators are used for the sub-ADC, the introduction and design of which can be found in [16]. The DZCD's output is used to switch off the current sources as previously stated in Sect. 4.1.1.

The current sources are implemented differently from [10] and based on the method suggested in [15] for current reuse and further power reduction. The switches S_5–S_6 are implemented using pMOS transistors as shown in Fig. 6(c) where SW3 is used as a dummy switch to match the current sources [15]. This structure is used for all stages except the first stage and the backend which are explained separately in the next sub-section. The shorting switches (S_1–S_4) are implemented using the bootstrapping technique described in [17].

4.1.3 First and last stage considerations

As the first stage samples the analog signal directly, there is no need to apply the current during its sampling phase. Therefore, the current sources will only be active during the charge transfer phase. This has been implemented as in [15] by using pMOS switches shown in Fig. 6(d). As no front-end sample and hold is used, the time constants of the MDAC and sub-ADC have to be matched. This is based on the on-resistance and parasitic capacitance of the sampling switches for both paths. As both paths use bootstrapped switches for sampling, and as the sampling capacitor for the sub-ADC have smaller capacitances than the stage capacitors, different bootstrapping circuit dimensions have to be used for the sub-ADC switches to match the time constants of the two paths.

The last stage is implemented as a 2-bit flash ADC. This stage only requires a sampling phase and there is no need

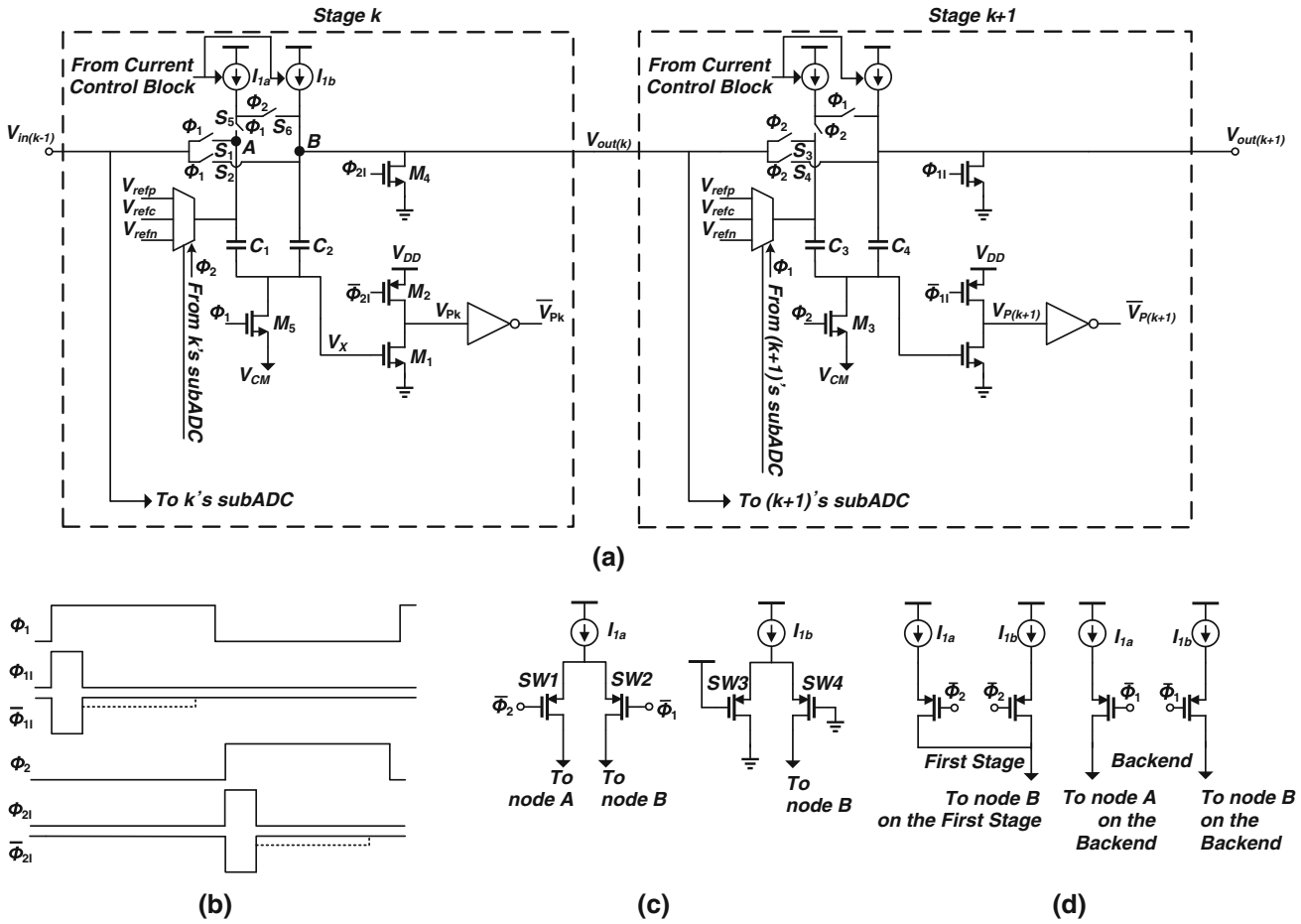

Fig. 6 Implementation of the proposed ADC: **a** general consecutive stages in the proposed design, **b** clock phases, **c** switches used to connect the current sources in *k*th stage, and **d** switches used to connect the current sources in the first stage and the backend

for a charge transfer phase. The backend is the 9th stage of the ADC, and therefore, it will be in sampling during ϕ_1 which is when the current sources need to be active. They can remain off during ϕ_2. To this end, the current sources for the backend are connected to the stage as shown in Fig. 6(d), using pMOS switches that are open during ϕ_2.

4.2 Multi-stage implementation

The proper manner to connect consecutive stages in order to create a pipeline ADC has already been depicted in Fig. 6(a). But, in order to efficiently use the CCBs for all stages, the following considerations are necessary.

Due to the fact that the CCB structures are identical for all stages and that only their inputs will change, there is the possibility of sharing them between consecutive stages. The current sources of any stage that is in its sampling phase need to be controlled by the V_X of its previous stage. In the same manner, any stage that is in the charge transfer phase has to be controlled by its own V_X. Based on this, Table 1 describes the controlling requirements of different stages during ϕ_1 and ϕ_2. As marked on Table 1, it can be seen that only four CCBs are needed during each phase and there is no need to have a separate CCB for each stage. By using the correct switching implementation, four CCBs will suffice to control the current of all stages. This will significantly reduce both the area and power consumption.

To implement this, the four CCBs need to be used as depicted in Fig. 7(a). The four control signals $V_{Ctrl1-4}$ need to be connected to the stages as shown in Fig. 7(b). In this manner, all the requirements described in Table 1 are met and the stages receive their required control signal at the right time. The preset phase, ϕ_{2I}, provides enough time for the switching action without affecting voltage nodes, as both V_X and V_{out} are reset during this phase and their values are not affected by the applied current.

Scaling was applied to the capacitors of consecutive stages with a factor of 0.5 until the 4th stage with the remaining stages having the same capacitances as the 4th stage, similar to the original design in [10], for a better comparison.

Table 1 Necessary control signals for CCBs used in different stages (Color table online)

	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	Backend
ϕ_1	Off	V_{X2}	V_{X2}	V_{X4}	V_{X4}	V_{X6}	V_{X6}	V_{X8}	V_{X8}
ϕ_2	V_{X1}	V_{X1}	V_{X3}	V_{X3}	V_{X5}	V_{X5}	V_{X7}	V_{X7}	Off

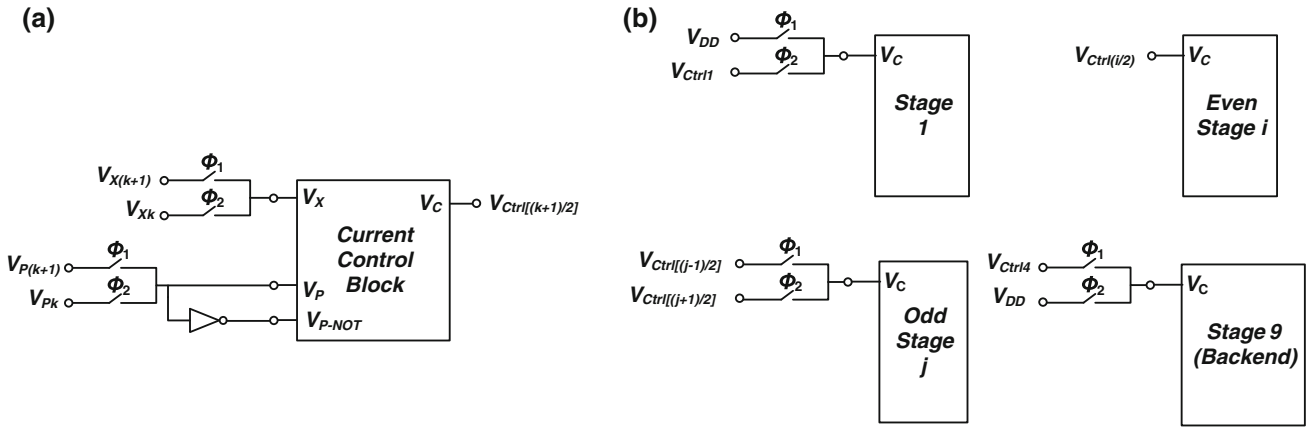

Fig. 7 Proposed CCB sharing technique: **a** creating the control signals and **b** applying the control signals to consecutive stages for proper CCB sharing

5 Simulation results

In order to verify the usefulness of the proposed ADC, Cadence circuit level simulation results are provided. For these simulations, the reference voltages V_{refp}, V_{refn} and V_{refc} were implemented ideally. The effects of circuit noise were simulated using PSS and PNoise analysis with a 'maxsideband' parameter of 500 in Cadence. The resulting input-referred sampled noise spectrum for the first stage is illustrated in Fig. 8. The integrated input-referred noise over the 100 kHz to 50 MHz bandwidth for stages 1–4 was 66.8, 69.2, 73.7 and 79 nV^2 respectively. Stages 5–9 will have an integrated input-referred noise similar to stage 4 equal to 79 nV^2, as their capacitors are not scaled further. The total converter input-referred noise is calculated using the following equation:

$$\bar{v}^2_{tot,in} = \bar{v}^2_{stage1,in} + \frac{\bar{v}^2_{stage2,in}}{A^2_{v1}} + \frac{\bar{v}^2_{stage3,in}}{A^2_{v1}A^2_{v2}} + \cdots + \frac{\bar{v}^2_{stage8,in}}{A^2_{v1} \times A^2_{v2} \times \cdots \times A^2_{v7}} \quad (3)$$

where A_{vi} is the ith stage gain and $\bar{v}^2_{stagej,in}$ is the integrated input-referred noise power for stage j. By substituting the terms in (3) with those listed above, the total converter input-referred noise is obtained as 90.35 nV^2 or −70.4 dB which is less than the converter LSB (−64.6 dB) obtained for $V_{\text{ref}} = 0.6$ V. This level of circuit noise was considered in SNDR calculations. To calculate the parameters SNDR and spurious free dynamic range (SFDR), 1,024-points FFT was utilized. The simulated ADC output spectrum for a sine wave single-ended input signal with 0.6 Vpp and 47.94921875 MHz frequency is shown in Fig. 9. The harmonic distortions visible in Fig. 9 are mainly because the opamp has been replaced by a less accurate alternative and also due to the circuit being single-ended. Calibration techniques could be used to compensate for the absence of the opamp and achieve a higher ENOB. It is worth mentioning that the original ZCBC structure [10], which is the basis for this work, is inherently single-ended.

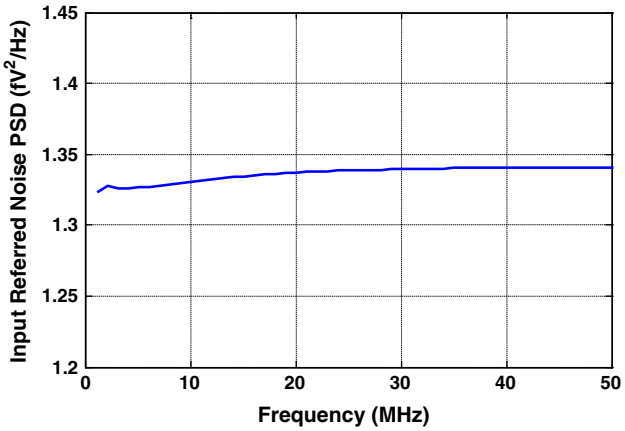

Fig. 8 First-stage input-referred noise spectrum

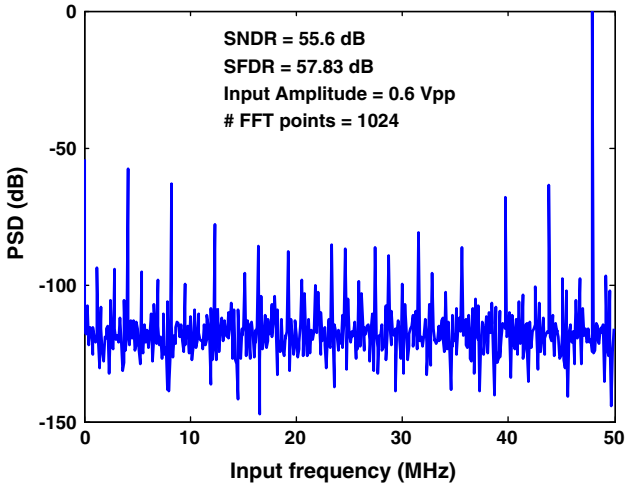

Fig. 9 Output spectrum excluding the circuit noise in TT @ 27 °C

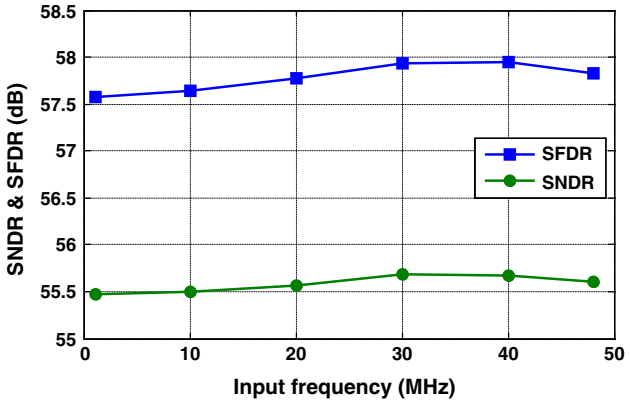

Fig. 10 Simulated SFDR and SNDR versus the input signal frequency

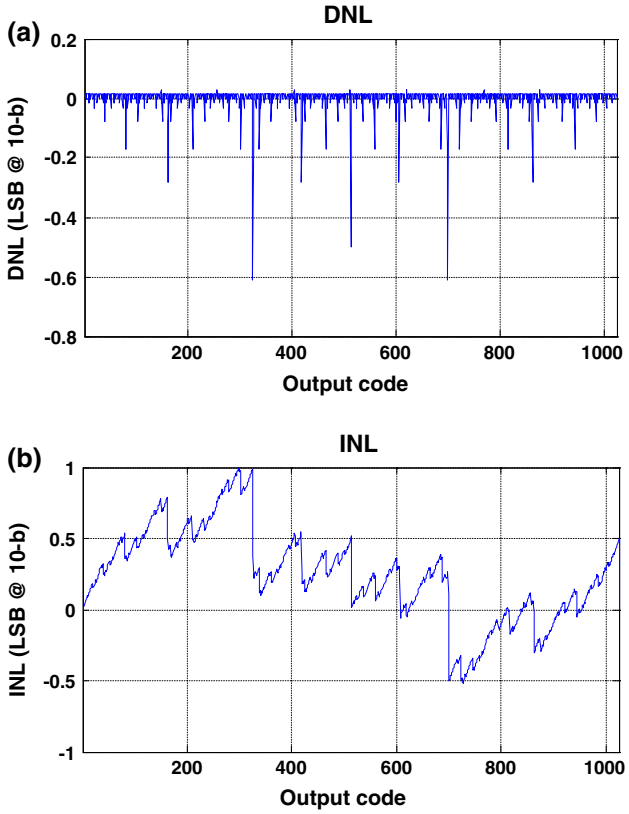

Fig. 11 Simulation results for **a** DNL and **b** INL in TT @ 27 °C

Table 2 Simulation results summary

Parameters	TT@ 27 °C	FF@ −40 °C	SS@ 85 °C
Technology	90 nm CMOS		
Resolution (bit)	10		
Sampling rate (MS/s)	100		
Supply voltage	1 V		
INL (LSB)	+0.99/−0.51		
DNL (LSB)	+0.03/−0.61		
SNDR (dB)	55.6	54.9	54.5
SFDR (dB)	57.8	57.6	58.2
Power dissipation (mW)	3.56	3.97	3.51
FoM (fJ/conv.step)	72.3	88	81.8

The simulated SNDR and SFDR versus the input signal frequency are plotted in Fig. 10. This figure shows variations of <0.5 dB for SFDR and <0.25 dB for SNDR for different input frequencies. Differential nonlinearity (DNL) and integral nonlinearity (INL) simulation results are shown in Fig. 11. The simulation results in different process corner cases and temperature variations are summarized in Table 2.

To evaluate the performance of the proposed ADC with several state-of-the-art implementations, the following FoM used in literature is employed:

$$FoM = \frac{Power}{f_S \times 2^{ENOB}} \quad (4)$$

where Power is the total ADC power consumption, f_s is the sampling frequency and ENOB is the effective number of bits. This FoM is a measure of the relation of overall power consumption over converter resolution and sampling frequency. The smaller the FoM value, the better the overall performance. The FoM for this work is obtained as 72.3 fJ/conv.step. Table 3 lists the performance of several recently published and prominent pipeline A/D converters. As is seen, this work is among the best published ones to date. It should be noted that although the reported results for the proposed ADC are based on Cadence simulation results, its outstanding FoM verifies its performance as a good candidate for low power applications.

Table 3 Performance comparison of the proposed ADC with several state-of-the-art converters

Reference	Process	Resolution (bit)	f_s (MS/s)	Method	SNDR (dB)	SFDR (dB)	Power (mW)	FoM (fJ/conv.step)
[This work][a]	90 nm	10	100	Controlled ZCBC	55.6	57.8	3.56	72.3
Microelectronics'12 [11]	0.18 μm	10	25	CBSC + Ch.pump	39.1	47	3.5	1,900
ISSCC'12 [18]	65 nm	10	200	Coarse/fine OTA	56.7	64	5.37	48
ISSCC'12 [19]	0.18 μm	10	30	Ring amp.	61.5	74.2	2.6	91
CICC'12 [20]	65 nm	13	40	ZCBC + SAR	59.5	70	4.5	142
JSSC'12 [21]	65 nm	12	30	ZCBC	66.7	87.4	5.96	112
AICSP'12 [22]	0.13 μm	10	60	OTA	56.84	65.64	23	670
VLSID'12 [23][a]	0.18 μm	8	300	OTA	49.08	57.40	55	789
MWSCAS'12 [24][a]	0.18 μm	10	250	OTA	61.84	78.1	30	140
ECCTD'11 [25][a]	90 nm	10	50	CCII	55.3	–	8.1	1,696
MWSCAS'11 [12][a]	90 nm	9	50	CBSC + TSCDS	50.76	–	3.65	259
ISCAS'11 [26][a]	0.13 μm	10	100	CBSC	58.8	70.4	5.9	81
MWSCAS'11 [27][a]	0.13 μm	10	10	Open-loop	44.5	–	5.5	401
ICECS'11 [28][a]	0.13 μm	10	40	OTA	56.04	64.4	3.9	188
AICSP'11 [29]	90 nm	8	60	CBSC	44.2	60	8.5	1,070
TCAS-II'11 [30]	90 nm	8	100	Current charge pump	37.1	46.7	1.39	238
IETCDS'11 [15]	0.18 μm	8	100	ZCBC	43.82	47.2	8	625
TCAS-I'11 [31]	90 nm	10	100	OTA	55	62.3	4.5	97
VLSIC'11 [32]	90 nm	10	320	Open-loop	52.93	–	40	345
JSSC'10 [13]	0.18 μm	11	20	OTA + ZCBC	68.2	76.5	17.1	390
AICSP'10 [33]	90 nm	8	125	OTA	39.4	45	9.4	840
TCAS-II'09 [14]	0.18 μm	8	20	Time domain ZCBC	44.2	50	4.64	3,501
JSSC'07 [10]	0.18 μm	8	100	ZCBC	43.3	–	4.5	377
JSSC'06 [9]	0.18 μm	10	7.9	CBSC	52	62	2.5	816
JSSC'03 [5]	0.35 μm	12	75	Open-loop	67	80	290	2,110

[a] Simulation results

6 Conclusions

A new charging method was proposed for zero-crossing based pipeline analog-to-digital converters. The charging currents are controlled by the error signal with the current levels getting reduced as the error signal becomes smaller. This causes the output signal to settle on its final value instead of continuing to ramp. This reduces the effect of the DZCD delay on the output signal and significantly improves the accuracy. The overall power consumption has also been reduced by controlling the applied current. The current controlling blocks were shared between consecutive stages to reduce the required area and power consumption. Extensive circuit level simulation results in the context of 10-bit, 100 MS/s pipeline ADC were provided verifying the usefulness of the proposed method.

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